20220256207

*FIG. 1*

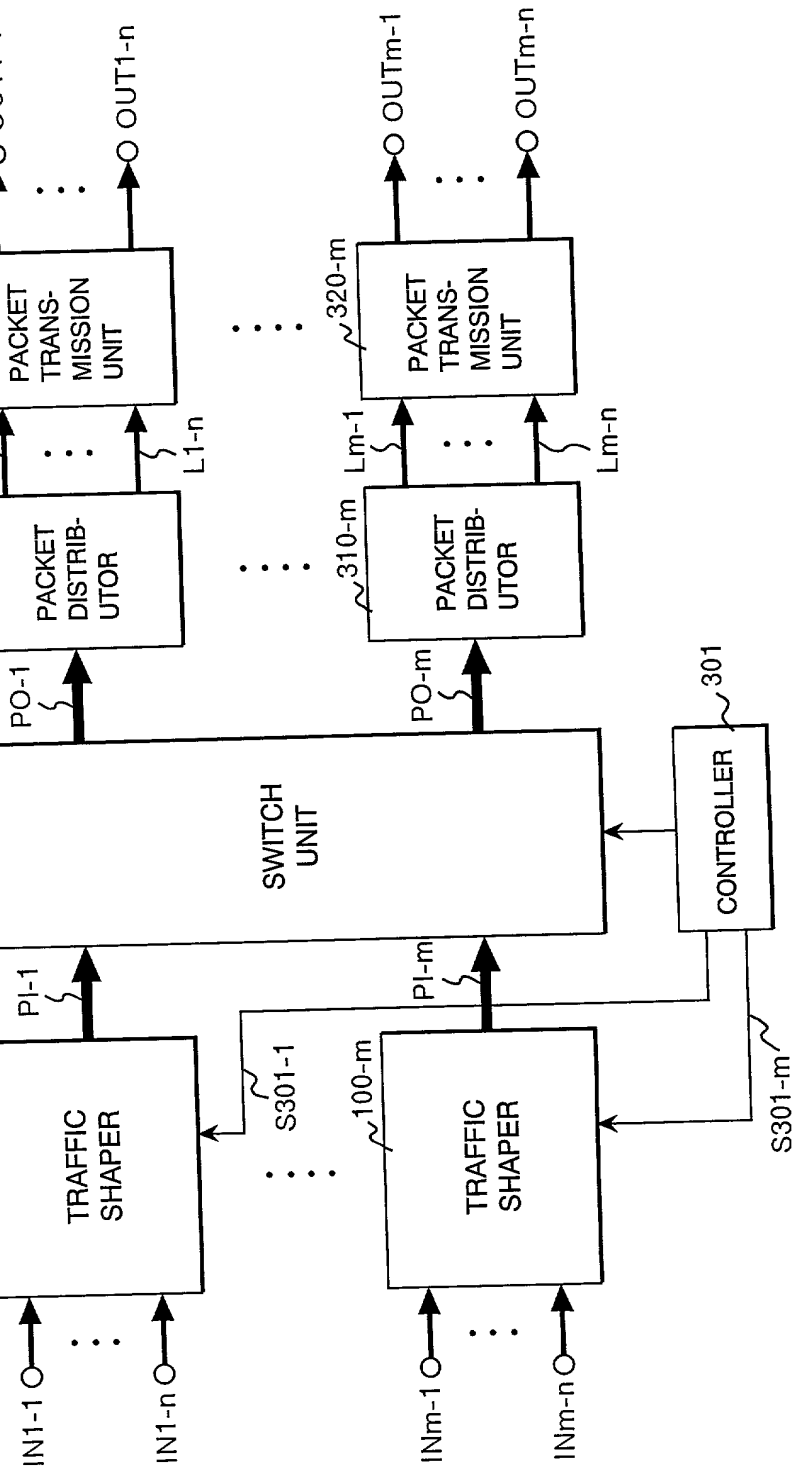


FIG. 2

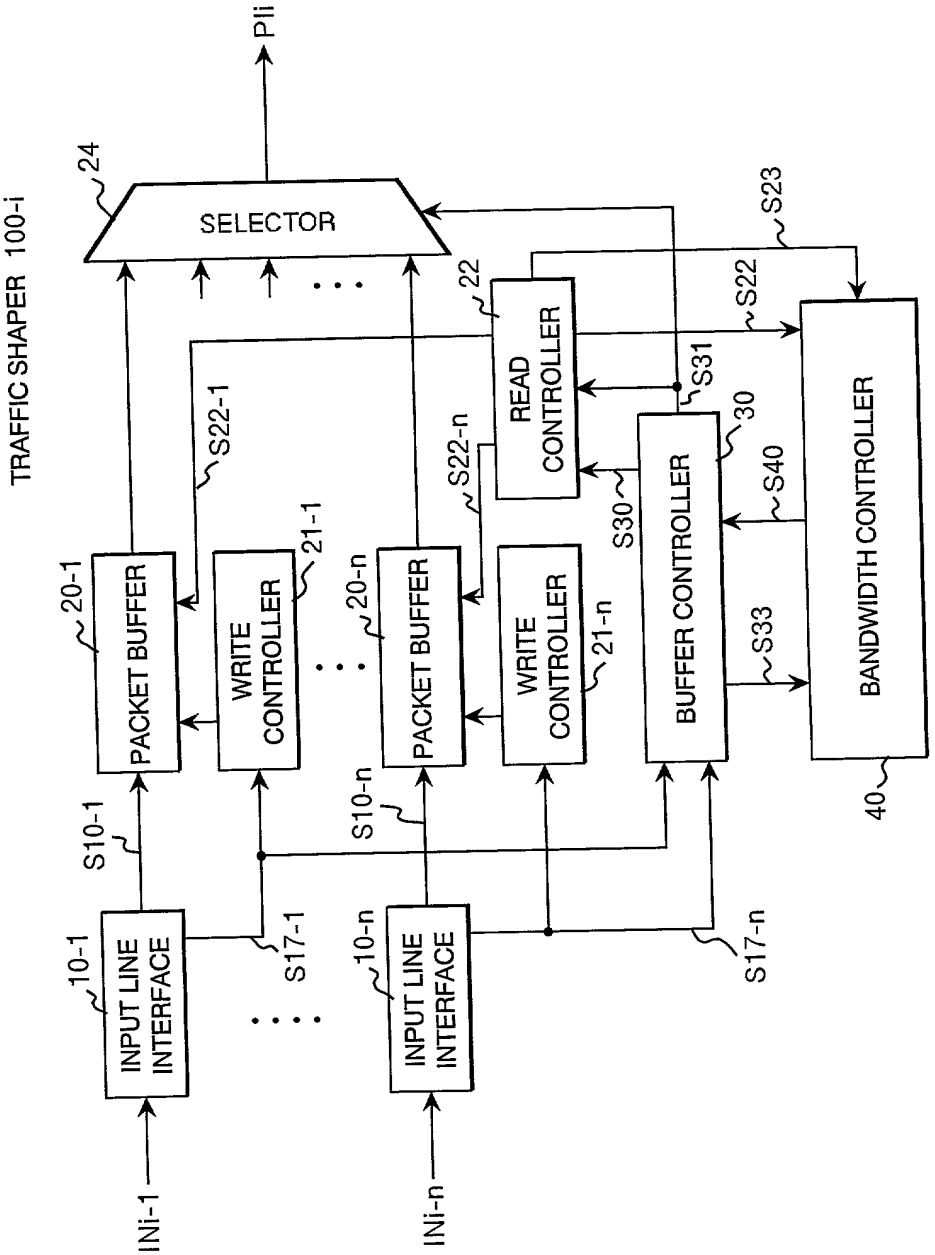
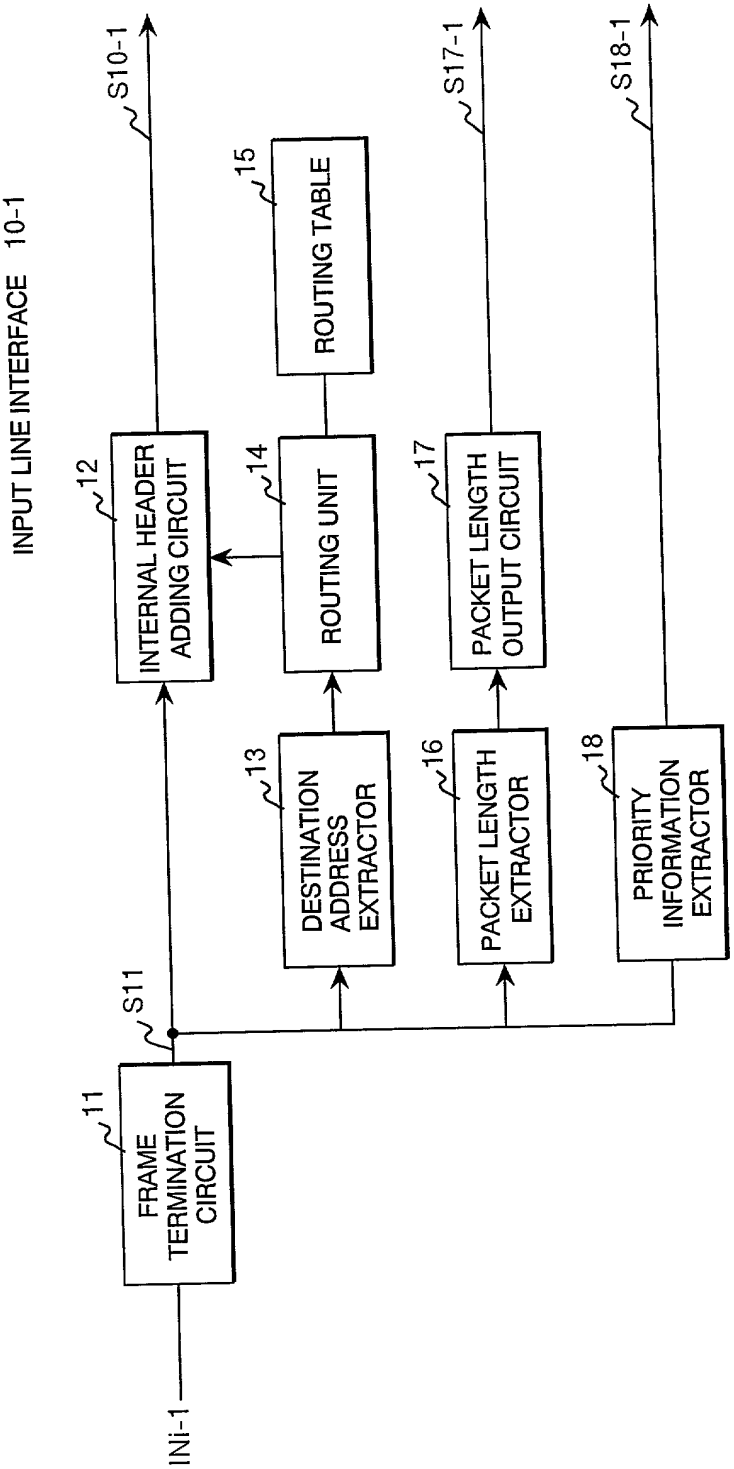
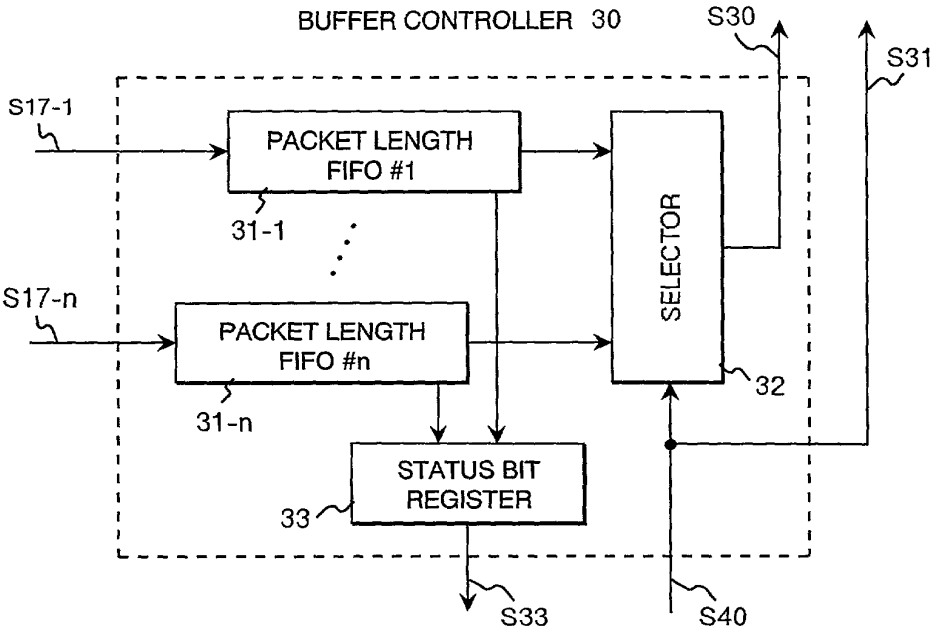

TRAFFIC SHAPER 100-i
SELECTOR
24
PIi
22
READ CONTROLLER
S23
S22
S31
30
S40
BUFFER CONTROLLER
BANDWIDTH CONTROLLER
40
S30
S33
20-1
PACKET BUFFER
21-1
WRITE CONTROLLER
S22-1
20-n
PACKET BUFFER
21-n
WRITE CONTROLLER
S22-n
S10-1
S10-n
10-1
INPUT LINE INTERFACE
10-n
INPUT LINE INTERFACE
S17-1
S17-n
INi-1
INi-n

*FIG. 3*


INPUT LINE INTERFACE 10-1
INi-1
11
FRAME TERMINATION CIRCUIT
S11
12
INTERNAL HEADER ADDING CIRCUIT
S10-1
13
DESTINATION ADDRESS EXTRACTOR
14
ROUTING UNIT
15
ROUTING TABLE
16
PACKET LENGTH EXTRACTOR
17
PACKET LENGTH OUTPUT CIRCUIT
S17-1
18
PRIORITY INFORMATION EXTRACTOR
S18-1

# FIG. 4


BUFFER CONTROLLER 30
S30
S31
S17-1
PACKET LENGTH FIFO #1
31-1
S17-n
PACKET LENGTH FIFO #n
31-n
SELECTOR
32
STATUS BIT REGISTER
33
S33
S40

# FIG. 5

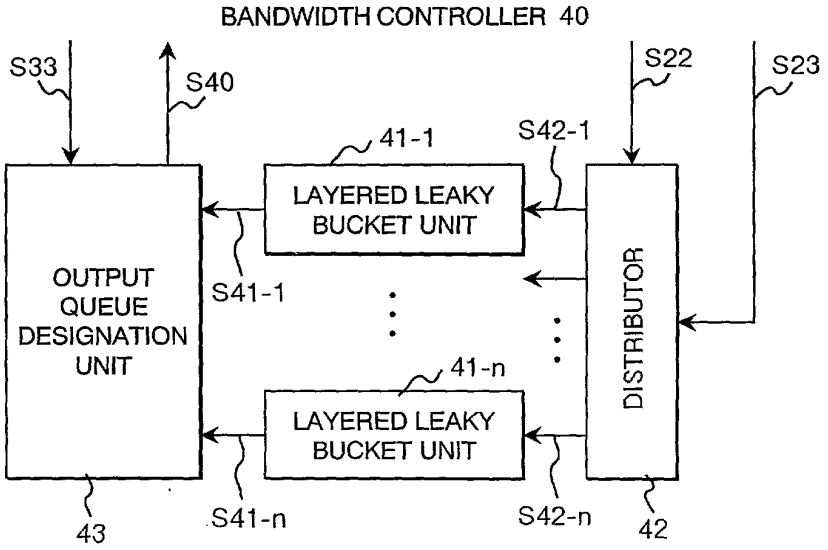

BANDWIDTH CONTROLLER 40
S33
S40
S22
S23
41-1
S42-1
LAYERED LEAKY BUCKET UNIT
OUTPUT QUEUE DESIGNATION UNIT
S41-1
DISTRIBUTOR
41-n
LAYERED LEAKY BUCKET UNIT
43
S41-n
S42-n
42

FIG. 6A

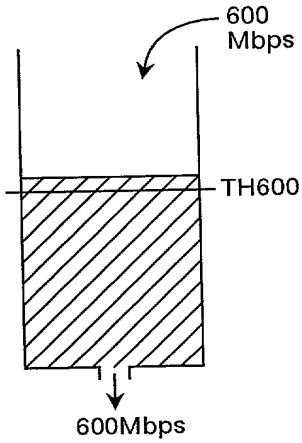



FIG. 6B

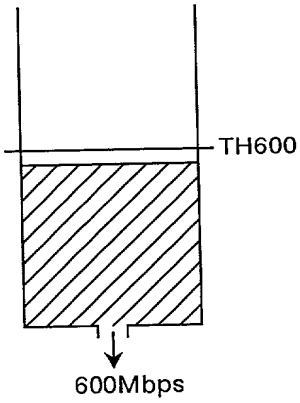



FIG. 6C

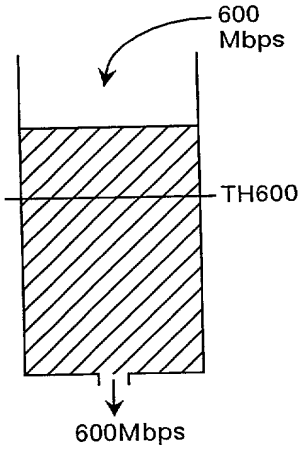



FIG. 6D

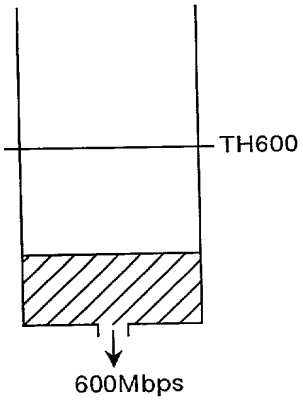



FIG. 6E

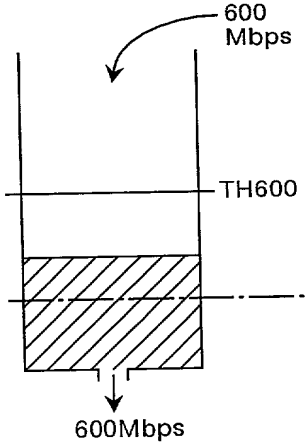
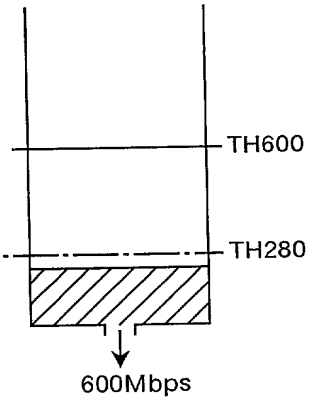



FIG. 6F

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# FIG. 7

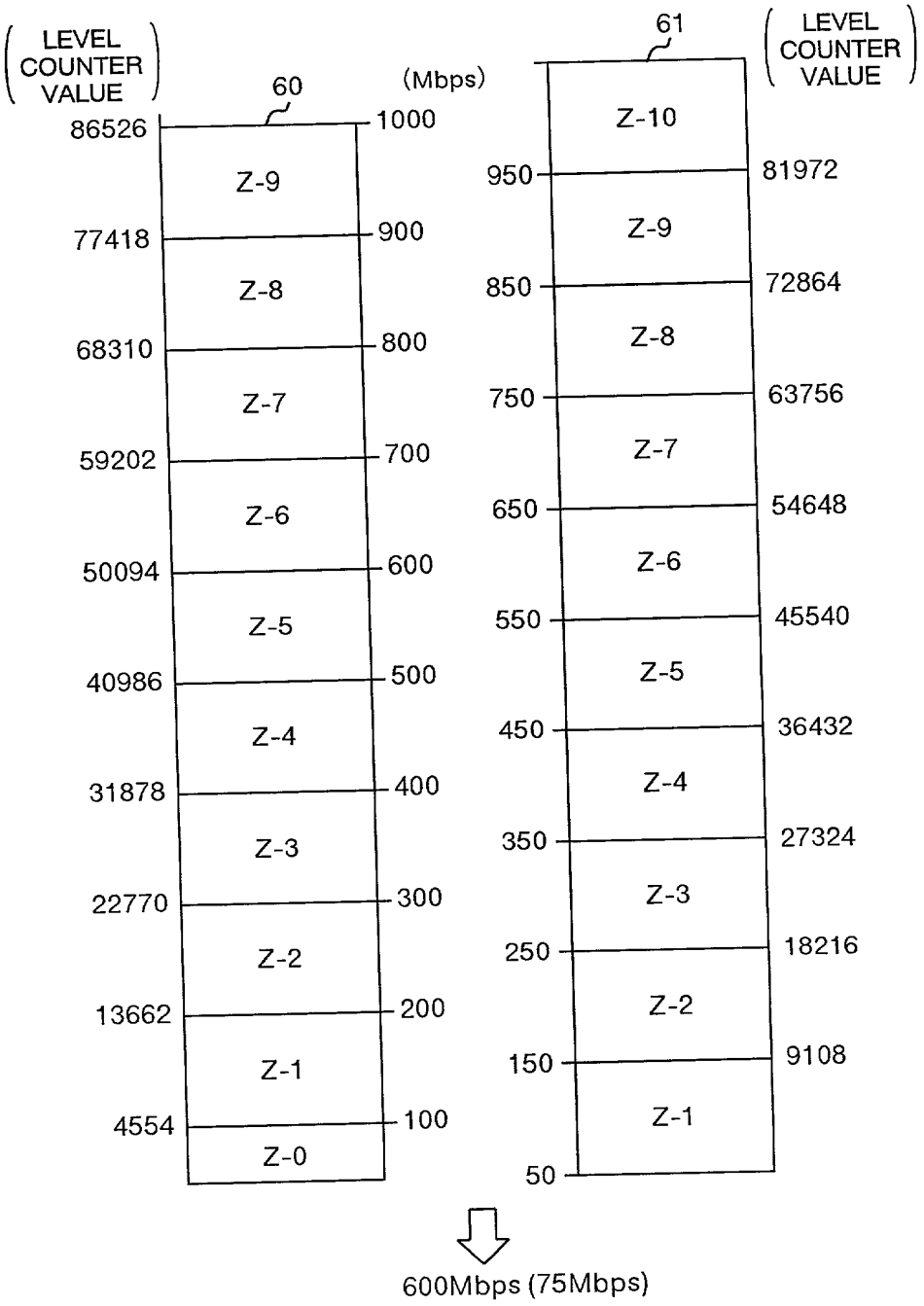

LEVEL COUNTER VALUE
60
(Mbps)
86526
1000
Z-9
77418
900
Z-8
68310
800
Z-7
59202
700
Z-6
50094
600
Z-5
40986
500
Z-4
31878
400
Z-3
22770
300
Z-2
13662
200
Z-1
4554
100
Z-0
61
LEVEL COUNTER VALUE
Z-10
950
81972
Z-9
850
72864
Z-8
750
63756
Z-7
650
54648
Z-6
550
45540
Z-5
450
36432
Z-4
350
27324
Z-3
250
18216
Z-2
150
9108
Z-1
50
600Mbps (75Mbps)

FIG. 8A

411

| LEVEL RANGE | $\alpha$ | |
|---|---|---|
| 86526 ~ | 6/10 | Z-10 |
| 77418 ~ 86525 | 6/9 | Z-9 |
| 68310 ~ 77417 | 6/8 | Z-8 |
| 59202 ~ 68309 | 6/7 | Z-7 |
| 50094 ~ 59201 | 1 | Z-6 |
| 40986 ~ 50093 | 6/5 | Z-5 |
| 31878 ~ 40985 | 6/4 | Z-4 |
| 22770 ~ 31877 | 2 | Z-3 |
| 13662 ~ 22769 | 3 | Z-2 |
| 4554 ~ 13661 | 6 | Z-1 |

FIG. 8B

412

| LEVEL RANGE | $\alpha$ | |
|---|---|---|
| 81972 ~ | 6/10 | Z-10 |
| 72864 ~ 81971 | 6/9 | Z-9 |
| 63756 ~ 72863 | 6/8 | Z-8 |
| 54648 ~ 63755 | 6/7 | Z-7 |
| 45540 ~ 54647 | 1 | Z-6 |
| 36432 ~ 45539 | 6/5 | Z-5 |
| 27324 ~ 36431 | 6/4 | Z-4 |
| 18216 ~ 27323 | 2 | Z-3 |
| 9108 ~ 18215 | 3 | Z-2 |
| 0 ~ 9107 | 6 | Z-1 |

FIG. 9

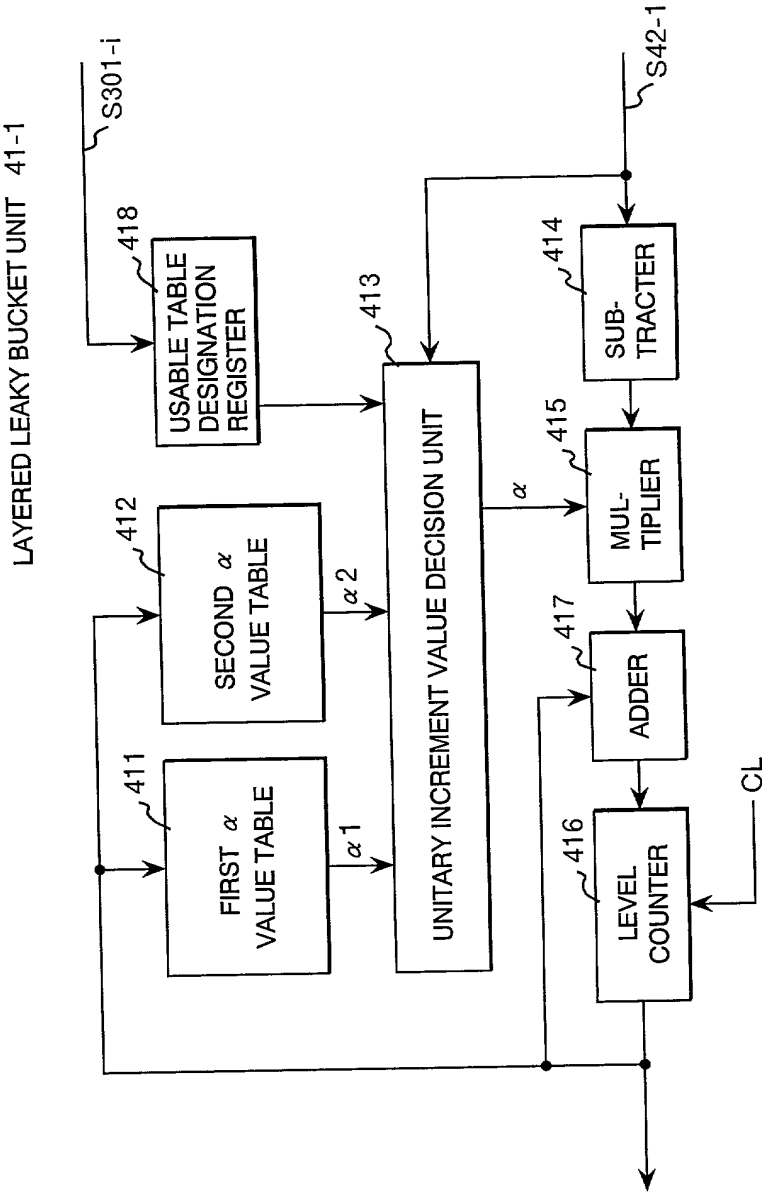

LAYERED LEAKY BUCKET UNIT 41-1
S301-i
418
USABLE TABLE DESIGNATION REGISTER
412
SECOND α VALUE TABLE
α2
411
FIRST α VALUE TABLE
α1
413
UNITARY INCREMENT VALUE DECISION UNIT
α
S42-1
414
SUB-TRACTER
415
MUL-TIPLIER
417
ADDER
416
LEVEL COUNTER
CL

FIG. 10

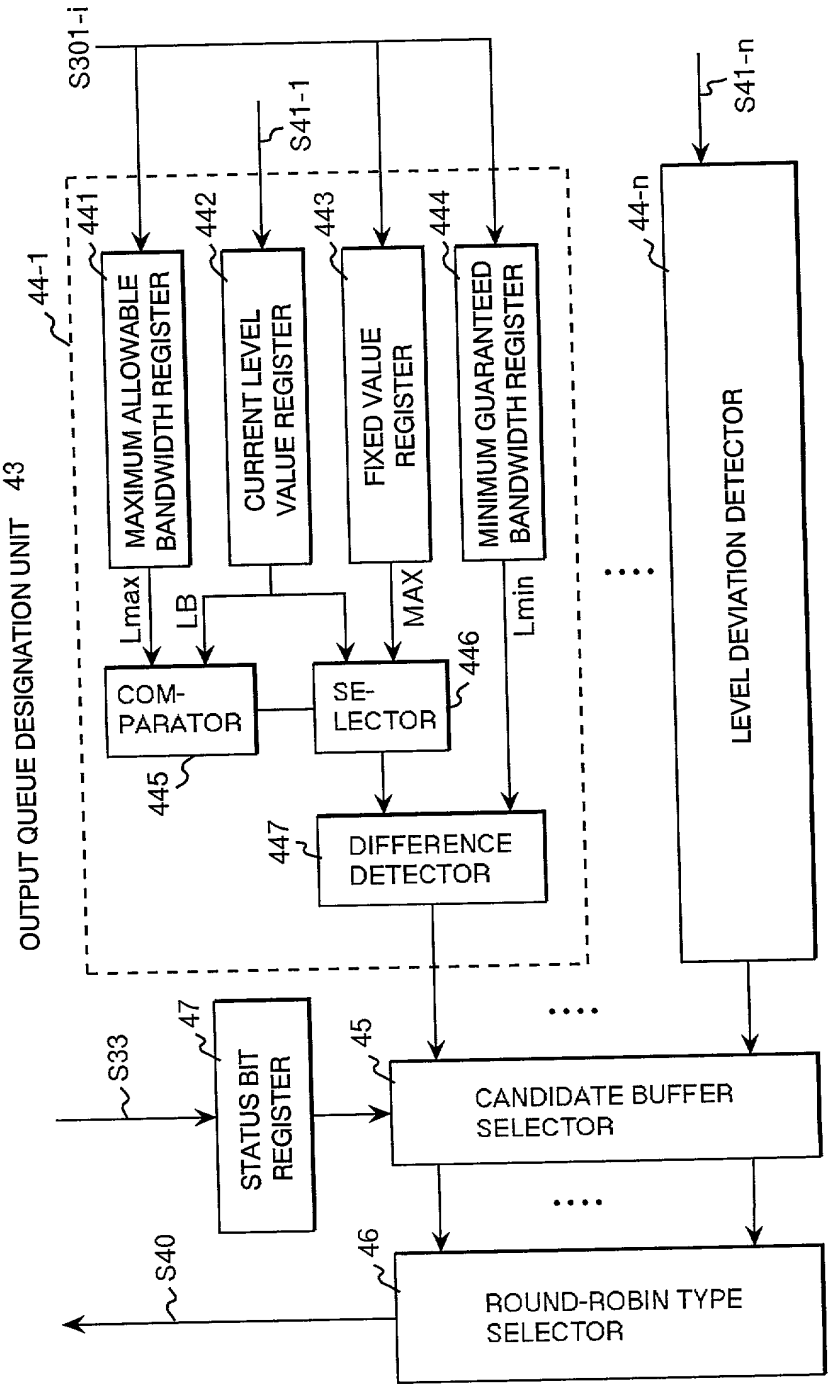

S301-i
S41-1
S41-n
44-1
441
442
443
444
44-n
MAXIMUM ALLOWABLE BANDWIDTH REGISTER
CURRENT LEVEL VALUE REGISTER
FIXED VALUE REGISTER
MINIMUM GUARANTEED BANDWIDTH REGISTER
LEVEL DEVIATION DETECTOR
OUTPUT QUEUE DESIGNATION UNIT 43
Lmax
LB
MAX
Lmin
COM-PARATOR
SE-LECTOR
446
445
447
DIFFERENCE DETECTOR
S33
47
STATUS BIT REGISTER
45
CANDIDATE BUFFER SELECTOR
S40
46
ROUND-ROBIN TYPE SELECTOR

FIG. 11

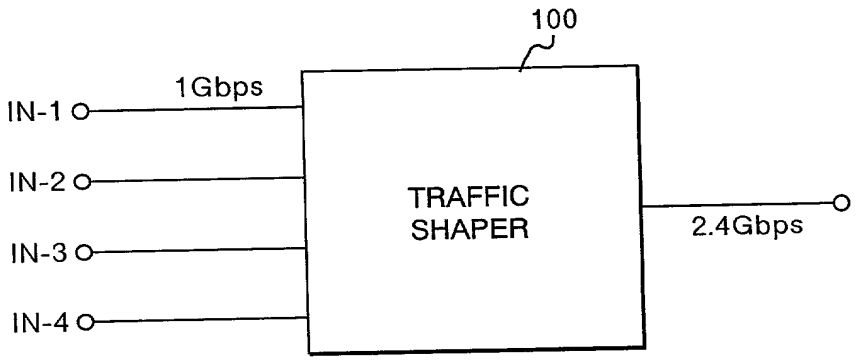


FIG. 12A

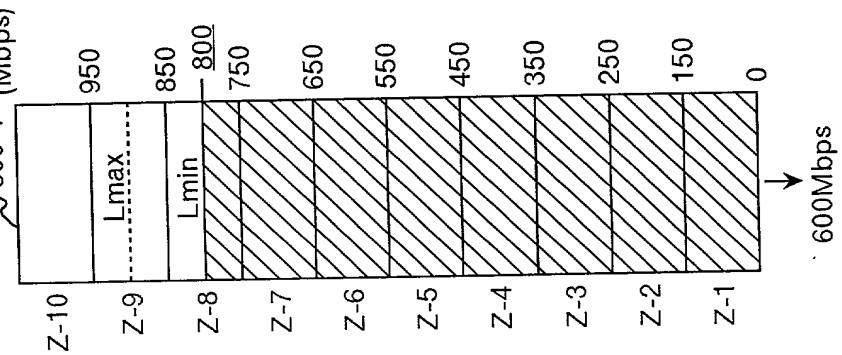



FIG. 12B

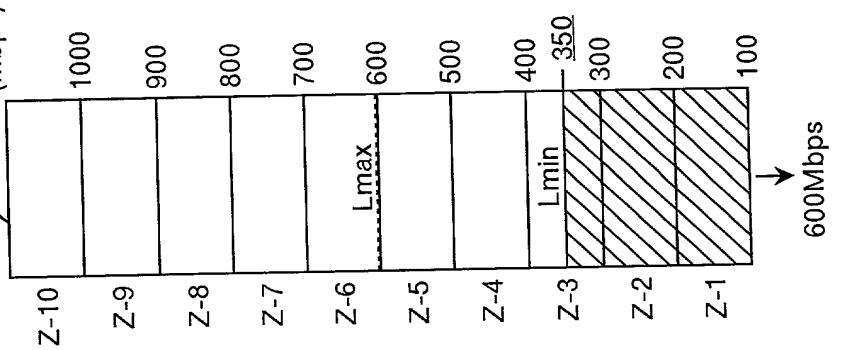



FIG. 12C

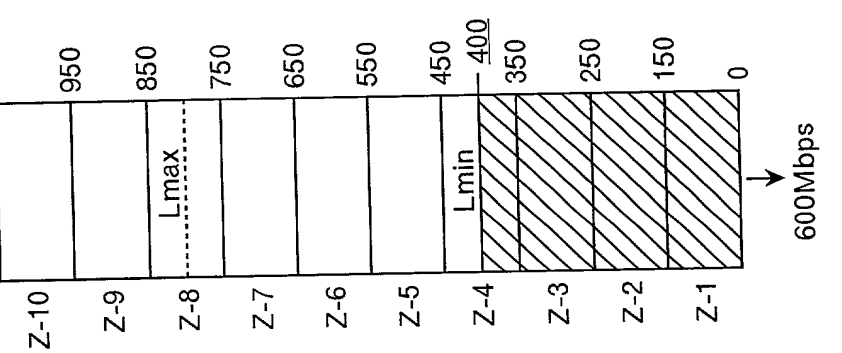



FIG. 12D

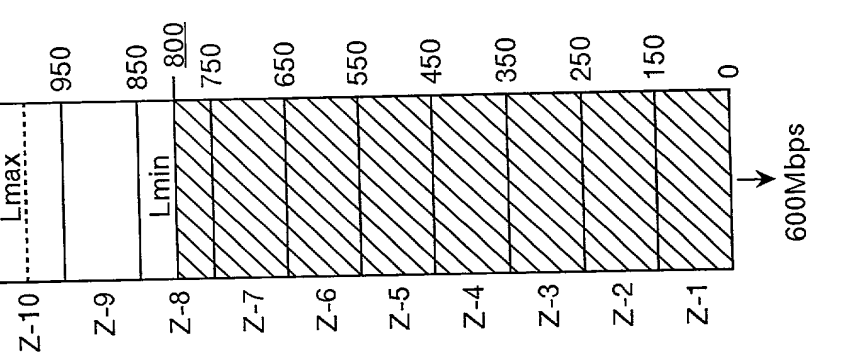


FIG. 13

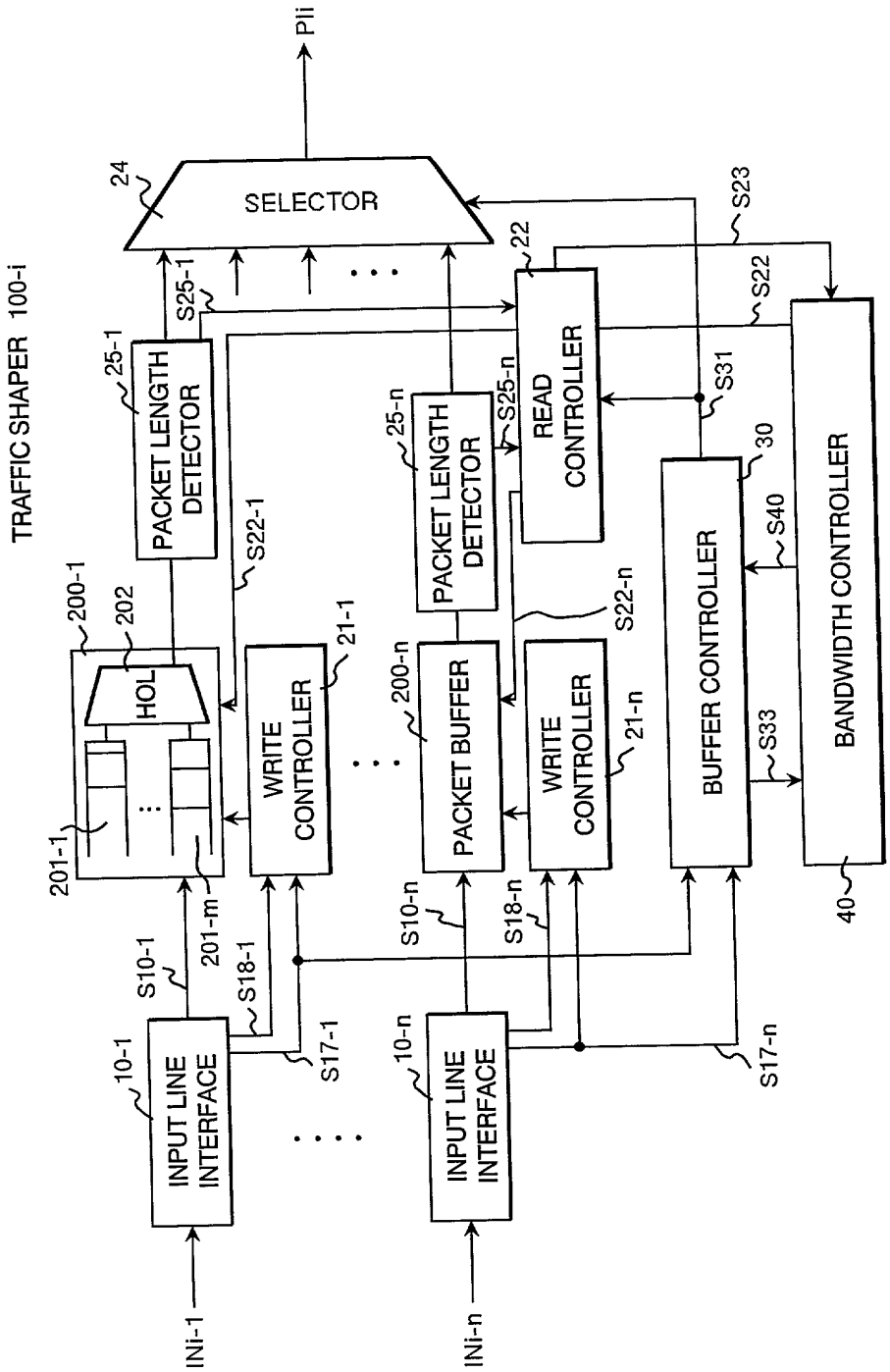

TRAFFIC SHAPER 100-i
INi-1
INi-n
INPUT LINE INTERFACE
10-1
10-n
S10-1
S10-n
S17-1
S17-n
S18-1
S18-n
201-1
201-m
200-1
200-n
202
HOL
WRITE CONTROLLER
21-1
21-n
PACKET BUFFER
PACKET LENGTH DETECTOR
25-1
25-n
S22-1
S22-n
S25-1
S25-n
READ CONTROLLER
22
SELECTOR
24
PIi
BUFFER CONTROLLER
30
S31
S40
S33
BANDWIDTH CONTROLLER
40
S22
S23

FIG. 14

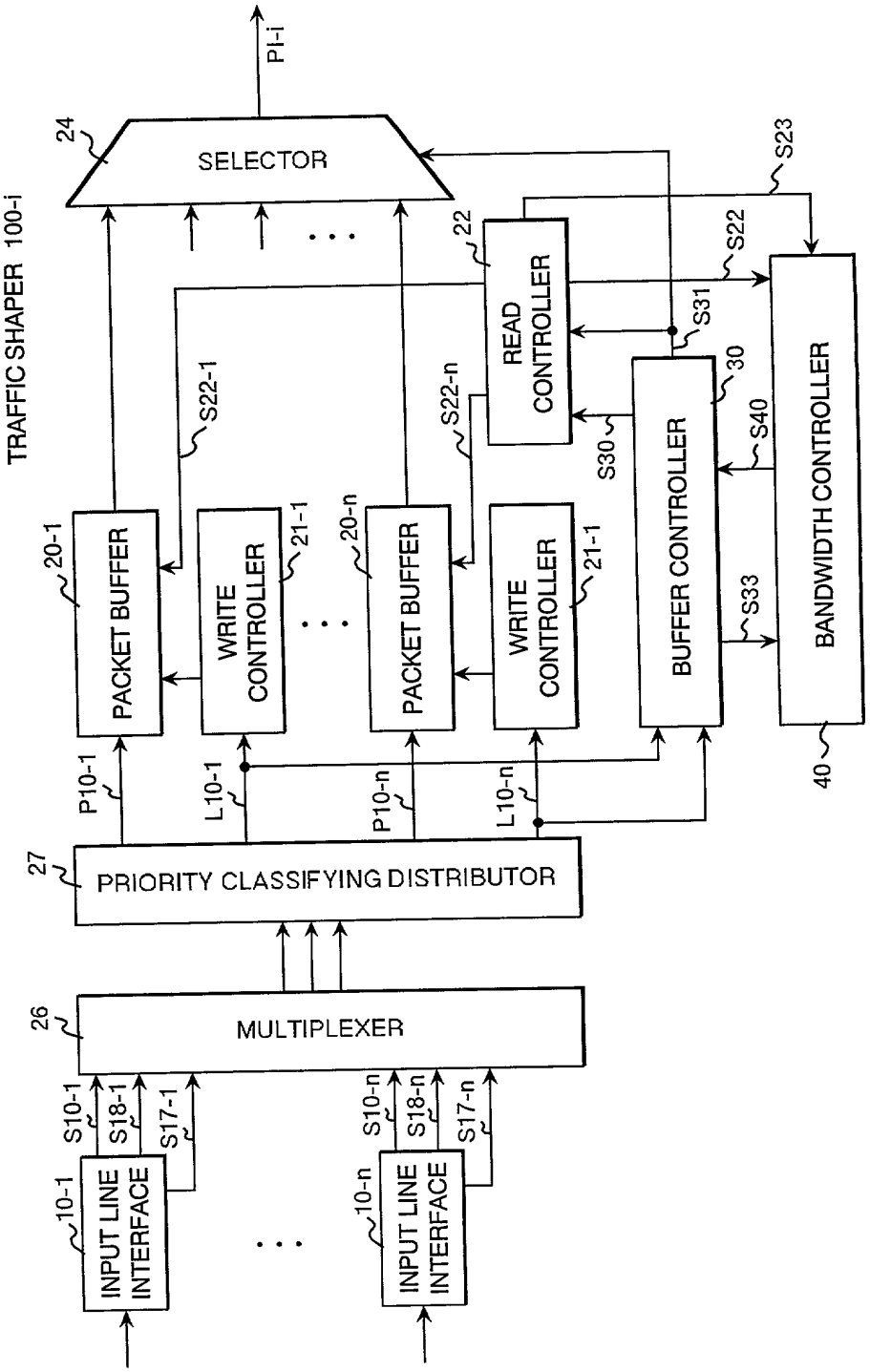
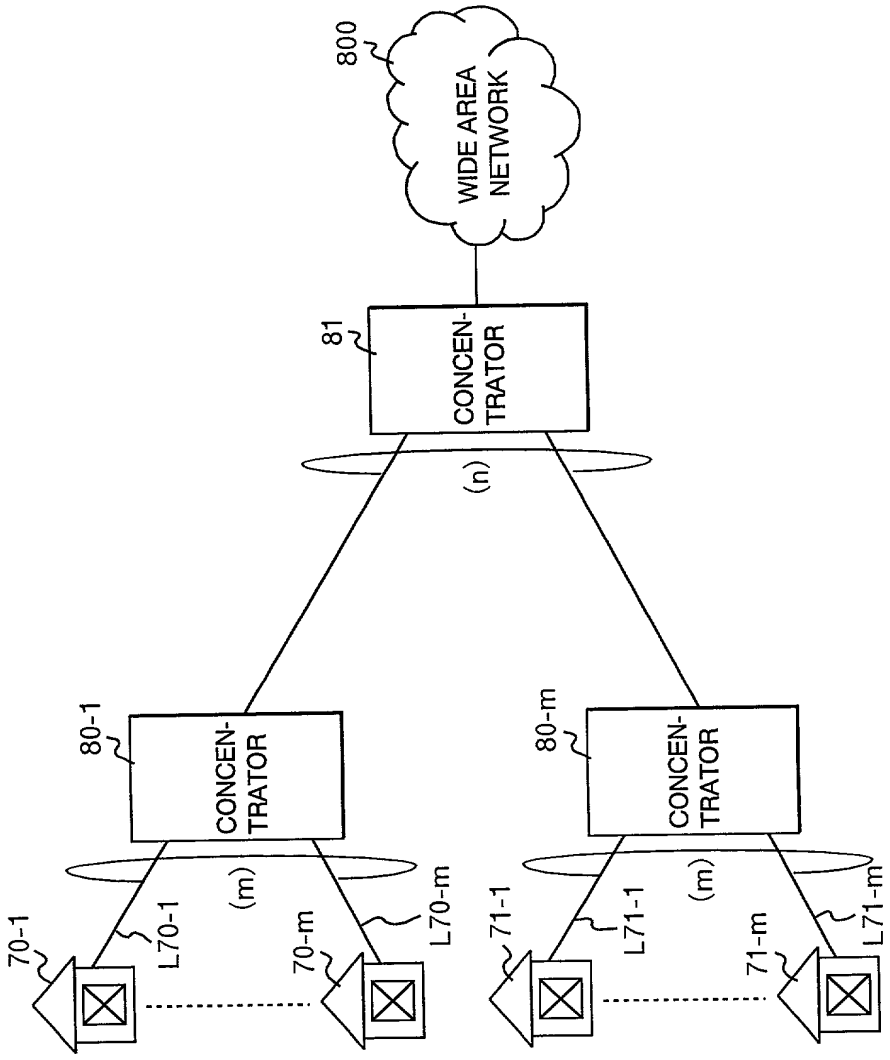

TRAFFIC SHAPER 100-i
PI-i
SELECTOR
24
S23
22
READ CONTROLLER
S22
S31
30
S40
BUFFER CONTROLLER
S30
BANDWIDTH CONTROLLER
40
S33
20-1
PACKET BUFFER
21-1
WRITE CONTROLLER
S22-1
20-n
PACKET BUFFER
21-1
WRITE CONTROLLER
S22-n
P10-1
L10-1
P10-n
L10-n
27
PRIORITY CLASSIFYING DISTRIBUTOR
26
MULTIPLEXER
S10-1
S18-1
S17-1
10-1
INPUT LINE INTERFACE
S10-n
S18-n
S17-n
10-n
INPUT LINE INTERFACE

FIG. 15


800
WIDE AREA NETWORK
81
CONCEN-TRATOR
(n)
80-1
CONCEN-TRATOR
80-m
CONCEN-TRATOR
(m)
(m)
70-1
L70-1
70-m
L70-m
71-1
L71-1
71-m
L71-m